WHAT IS CLAIMED IS:

1. A semiconductor structure used in manufacturing a semiconductor device, comprising:

a substrate layer;

first and second isolation regions formed by etching an oxide layer provided on the substrate layer to define an epitaxial growth surface of the substrate layer for epitaxial growth of a substrate material on the epitaxial growth surface between the first and second isolation regions; and

an active region comprising the epitaxially-grown substrate material between the first and second isolation regions, the active region formed by epitaxially growing the substrate material on the epitaxial growth surface of the substrate layer.

2. The structure of Claim 1, wherein the isolation regions and the active region are formed independent of any shallow trench isolation (STI) process in which an isolation region is formed by etching a trench in the substrate layer and filling the trench with an oxide material to define an adjacent active region of the structure.

3. The structure of Claim 1, wherein the epitaxially-grown substrate material comprises dopant material introduced into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the epitaxial growth surface of the substrate layer.

4. The structure of Claim 1, wherein:

the active region comprises a first active region, the epitaxially-grown substrate material of the first active region comprising a first dopant material introduced into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the first epitaxial growth surface of the substrate layer; and

the structure further comprises:

a third isolation region formed by etching the oxide layer provided on the substrate layer to define a second epitaxial growth surface of the substrate layer for epitaxial growth of the substrate material on the second epitaxial growth surface between the second and third isolation regions, the second epitaxial growth surface of the substrate layer having been masked while the epitaxially-grown substrate material was grown and the first dopant material was introduced on the first epitaxial growth surface of the substrate layer; and

a second active region comprising the epitaxially-grown substrate material between the second and third isolation regions, the second active region formed by epitaxially growing the substrate material on the second epitaxial growth surface of the substrate layer, the epitaxially-grown substrate material of the second active region comprising a second dopant material introduced into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the second epitaxial growth surface of the substrate layer while the first active region is masked.

5. The structure of Claim 1, wherein the structure has been formed substantially independent of:

an implant process for introducing a dopant material into the active region; and

an anneal process for activating the dopant material.

6. The structure of Claim 1, wherein:

the device comprises a complementary metal oxide semiconductor (CMOS) device; and

the epitaxially-grown substrate material forms at least one of a p-type well and an n-type well underlying the active region.

7. The structure of Claim 1, further comprising a transistor comprising:

a pad layer provided on the active region;

a gate formed on the pad layer;

a substantially vertical isolation layer formed on each side of the gate and adapted to laterally isolate the gate; and

an extender epitaxially grown on the active region on each side of the gate, the isolation layer on each side of the gate laterally isolating the gate from the corresponding extender, each extender comprising either a p-type material or an n-type material and adapted to serve as either a source or a drain for the transistor.

8. The structure of Claim 7, wherein the source and the drain of the transistor are formed independent of any process for implanting either a p-type material or an n-type material into the active region.

9. The structure of Claim 7, wherein:

the isolation layers formed on each side of the gate comprise first isolation layers each having a first length; and

the extenders epitaxially grown on the active region on each side of the gate comprise first extenders each having a first length;

the structure further comprising:

a second substantially vertical isolation layer formed on each side of the gate and adapted to further isolate the gate, the second isolation layers each having a second length that is less than the first length of an adjacent first isolation layer;

a second extender epitaxially grown on the first extender on each side of the gate, each second extender comprising either a p-type material or an n-type material and adapted to serve as either a source or a drain for the transistor.

10. A semiconductor structure used in manufacturing a complementary metal oxide semiconductor (CMOS) device, comprising:

a substrate layer;

first and second isolation regions formed by etching an oxide layer provided on the substrate layer to define an epitaxial growth surface of the substrate layer for epitaxial growth of a substrate material on the epitaxial growth surface between the first and second isolation regions; and

an active region comprising the epitaxially-grown substrate material between the first and second isolation regions, the active region formed by epitaxially growing the substrate material on the epitaxial growth surface of the substrate layer, the epitaxially-grown substrate material forms at least one of a p-type well and an n-type well underlying the active region, the epitaxially-grown substrate material comprising dopant material introduced into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the epitaxial growth surface of the substrate layer;

the isolation regions and the active region formed independent of any shallow trench isolation (STI) process in which an isolation region is formed by etching a trench in the substrate layer and filling the trench with an oxide material to define an adjacent active region of the structure;

the structure formed substantially independent of:

an implant process for introducing a dopant material into the active region; and

an anneal process for activating the dopant material.

11. The structure of Claim 10, further comprising a transistor comprising:

a pad layer provided on the active region;

a gate formed on the pad layer;

a substantially vertical isolation layer formed on each side of the gate and adapted to laterally isolate the gate; and

an extender epitaxially grown on the active region on each side of the gate, the isolation layer on each side of the gate laterally isolating the gate from the corresponding extender, each extender comprising either a p-type material or an n-type material and adapted to serve as either a source or a drain for the transistor, the source and the drain formed independent of any process for implanting either a p-type material or an n-type material into the active region.

12. A method for forming a semiconductor structure in manufacturing a semiconductor device, comprising:

providing a substrate layer;

etching an oxide layer provided on the substrate layer to form first and second isolation regions, the first and second isolation regions defining an epitaxial growth surface of the substrate layer for epitaxial growth of a substrate material on the epitaxial growth surface between the first and second isolation regions; and

epitaxially growing the substrate material on the epitaxial growth surface of the substrate layer to form an active region comprising the epitaxially-grown substrate material between the first and second isolation regions.

13. The method of Claim 12, comprising forming the isolation regions and the active region independent of any shallow trench isolation (STI) process in which an isolation region is formed by etching a trench in the substrate layer and filling the trench with an oxide material to define an adjacent active region of the structure.

14. The method of Claim 12, further comprising introducing a dopant material into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the epitaxial growth surface of the substrate layer, the epitaxially-grown substrate material comprising the dopant material.

15. The method of Claim 12, wherein the active region comprises a first active region, the method further comprising:

introducing a first dopant material into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the epitaxial growth surface of the substrate layer to for the first active region, the epitaxially-grown substrate material comprising the first dopant material;

etching the oxide layer provided on the substrate layer to form a third isolation region, the third isolation region defining a second epitaxial growth surface of the substrate layer for epitaxial growth of the substrate material on the second epitaxial growth surface between the second and third isolation regions, the second epitaxial growth surface of the substrate layer having been masked while the epitaxially-grown substrate material was grown and the first dopant material was introduced on the first epitaxial growth surface of the substrate layer; and

epitaxially growing the substrate material on the second epitaxial growth surface of the substrate layer to form a second active region comprising the epitaxially-grown substrate material between the second and third isolation regions, the epitaxially-grown substrate material of the second active region comprising a second dopant material introduced into the epitaxially-grown substrate material as the epitaxially-grown substrate material is grown on the second epitaxial growth surface of the substrate layer while the first active region is masked.

16. The method of Claim 12, comprising forming the structure substantially independent of:

an implant process for introducing a dopant material into the active region; and

an anneal process for activating the dopant material.

17. The method of Claim 12, wherein:

the device comprises a complementary metal oxide semiconductor (CMOS) device; and

the epitaxially-grown substrate material forms at least one of a p-type well and an n-type well underlying the active region.

18. The method of Claim 12, further comprising a transistor, forming the transistor comprising:

providing a pad layer on the active region;

forming a gate on the pad layer;

forming a substantially vertical isolation layer on each side of the gate, the substantially vertical isolation layers adapted to laterally isolate the gate; and

epitaxially growing an extender on the active region on each side of the gate, the isolation layer on each side of the gate laterally isolating the gate from the corresponding extender, each extender comprising either a p-type material or an n-type material and adapted to serve as either a source or a drain for the transistor.

19. The method of Claim 18, comprising forming the source and the drain of the transistor independent of any process for implanting either a p-type material or an n-type material into the active region.

20. The method of Claim 18, wherein:

the isolation layers formed on each side of the gate comprise first isolation layers each having a first length; and

the extenders epitaxially grown on the active region on each side of the gate comprise first extenders each having a first length;

the method further comprising:

forming a second substantially vertical isolation layer on each side of the gate and adapted to further isolate the gate, the second isolation layers each having a second length that is less than the first length of an adjacent first isolation layer;

epitaxially growing a second extender on the first extender on each side of the gate, each second extender comprising either a p-type material or an n-type material and adapted to serve as either a source or a drain for the transistor.